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YAROSLAV BURKOVSKIY
National Technical University of Ukraine «Igor Sikorsky Kyiv Polytechnic Institute»
https://orcid.org/0000-0003-0633-1911
e-mail: yaroslav0590@gmail.com
YURIY ZINKOVSKIY
National Technical University of Ukraine «Igor Sikorsky Kyiv Polytechnic Institute»
https://orcid.org/0000-0003-4234-3549
e-mail: yuzin@ukr.net

POWER LOSS CHARACTERIZATION IN COMPACT GAN TRANSISTOR-BASED SYNCHRONOUS BUCK CONVERTERS FOR AERIAL DRONE APPLICATIONS

This article presents a comprehensive analysis of power loss in compact Gallium Nitride (GaN) transistor-based synchronous buck converters, specifically tailored for aerial drone applications (UAV). The study begins by outlining the increasing demand for efficient power management in drones, driven by the need for longer flight times and enhanced performance. The focus then shifts to the utilization of GaN transistors, highlighting their advantages over traditional silicon-based components in terms of efficiency, size, and thermal performance.

The core of the research involves an examination of power loss mechanisms in these converters. This includes both conduction and switching losses, with a particular emphasis on how the unique properties of GaN transistors influence these factors. The methodology adopted for this analysis combines theoretical modeling with empirical data.

Subsequently, the article delves into the design considerations for optimizing these converters. It discusses the balancing act between minimizing power loss and maintaining other critical parameters, such as size, weight, and cost. Practical strategies for achieving this balance are explored, including circuit design optimizations and the selection of appropriate ancillary components.

The findings of this study are significant for engineers and designers in the field of power electronics, particularly those working on aerial drone technology. The solutions provided into the GaN transistor-based synchronous buck converters under real-world conditions offer valuable guidelines for enhancing the efficiency and performance of these systems. Furthermore, the research contributes to the broader understanding of GaN technology in power applications, reinforcing its potential as a superior alternative to traditional silicon solutions.

In conclusion, this article not only provides an analysis of the specific area of power loss in GaN-based converters for drones but also underscores the broader implications and benefits of this technology in advancing the capabilities of power electronic systems.

Keywords: synchronous buck converter, gallium nitride, GaN, UAV, power management, calculation.

БУРКОВСЬКИЙ ЯРОСЛАВ, ЗІНЬКОВСЬКИЙ ЮРІЙ
Національний технічний університет України «Київський політехнічний інститут імені Ігоря Сікорського»

МЕТОДИКА ОЦІНКИ ВТРАТ У СИНХРОННИХ ПОНИЖУЮЧИХ ПЕРЕТВОРЮВАЧАХ СИСТЕМ ЖИВЛЕННЯ БПЛА НА ОСНОВІ GAN ТРАНЗИСТОРІВ

У цій статті представлено комплексний аналіз втрат потужності в транзисторних синхронних понижуючих перетворювачах на основі нітриду галію (GaN), спеціально розроблених для використання в безпілотних літальних апаратах (БПЛА). Дослідження починається з окреслення зростаючого попиту на ефективне управління живленням у безпілотних літальних апаратах, обумовленого потребою в більш тривалому польоті та покращені характеристик, а також аналізу використання GaN транзисторів, підкреслюючи їхні переваги перед традиційними рішеннями на основі кремнію з точки зору ефективності, розміру та теплових характеристик.

Основою дослідження є вивчення механізмів втрати потужності в цих перетворювачах. Це включає втрати як на провідність, так і на комутацію, з оцінкою того, як властивості GaN транзисторів впливають на ці фактори. Методологія, прийнята для цього аналізу, поєднує теоретичне моделювання з емпіричними даними.

Згодом у статті розглядаються конструктивні міркування для оптимізації цих перетворювачів. У ньому обговорюється балансування між мінімізацією втрат електроенергії та збереженням інших критичних параметрів, таких як розмір, вага та вартість. Вивчаються практичні стратегії для досягнення цього балансу, включаючи оптимізацію схеми та вибір відповідних допоміжних компонентів.

Результати цього дослідження є важливими для інженерів у галузі силової електроніки, особливо тих, хто працює над технологіями систем живлення БПЛА. Рішення, використані в синхронних понижуючих перетворювачах на основі GaN транзисторів в реальних умовах, пропонують цінні рішення для підвищення ефективності подібних систем живлення. Крім того, дослідження сприяє ширшому розумінню технології GaN в силовій електроніці, демонструючи її потенціал як кращої альтернативи традиційним кремнієвим рішенням.

У підсумку, ця стаття не тільки містить аналіз конкретної області втрат потужності в перетворювачах на основі GaN для БПЛА, але також підкреслює ширші переваги цієї технології в розширенні можливостей систем живлення.

Ключові слова: синхронний понижуючий перетворювач, нітрид галію, GaN, БПЛА, керування живленням, розрахунок.

Introduction

In the rapidly evolving landscape of UAV technology, the search for enhanced efficiency and performance has become an essential task. Central to this goal is the development of advanced power management systems, capable of meeting the strict demands of extended flight times and robust operational capabilities. This paper focuses on a critical component of these systems: the power converters. Specifically, we examine the application of compact Gallium Nitride (GaN) transistor-based synchronous buck converters in drones, a choice driven by the need for high efficiency and a lightweight in a compact form factor.

Gallium Nitride, a semiconductor material that has gained significant attention in recent years, offers several advantages over traditional silicon in power electronics. These advantages include higher efficiency, faster switching speeds, and better thermal management — attributes that are particularly beneficial in the constrained spaces and demanding thermal environments of aerial drones [1]. The adoption of GaN transistors in synchronous buck converters, a common type of voltage regulator, promises not only to enhance power efficiency but also to reduce the size and weight of the power management system, a critical consideration in UAV design [2].

However, the integration of GaN transistors into these converters is not without its challenges. One of the primary concerns is the characterization and optimization of power loss. Power loss in converters not only affects efficiency but also impacts heat generation, a critical factor in compact and thermally constrained spaces [3]. Understanding and minimizing these losses is crucial for the practical application of GaN transistor-based converters.

This paper presents a comprehensive analysis of power loss in these converters, focusing on both conduction and switching losses. The study employs a blend of theoretical modeling and empirical data, gathered under various operational conditions to simulate real-world applications. The insights gained from this analysis are then applied to explore design strategies for optimizing these converters, balancing the trade-offs between efficiency, size, cost, and complexity.

Tasks of the research

Through this research, we aim to provide a detailed understanding of the loss calculation in GaN-based synchronous buck converters. This work not only contributes to the field of power electronics in UAVs but also offers broader insights into the application of GaN transistors in different power systems.

Main research

Synchronous buck converters are widely employed for voltage step-down applications, converting higher input voltages to lower output levels. A fundamental schematic of this system is depicted in Figure 1. The operational principle of the converter can be described as follows: The Q1 MOSFET is connected to the input voltage source. Upon activation of Q1, current flows from the input to the output, leading to an increase in the L1 inductor current and consequent energy storage within the inductor. During this phase, the Q2 MOSFET remains inactive. Conversely, when Q1 is deactivated and Q2 is activated, the current traverses through Q2 in the opposite direction. This results in a decrease in the inductor current, facilitating the transfer of some of the stored energy in the inductor to the load. Figure 2 illustrates the basic waveforms associated with this process.

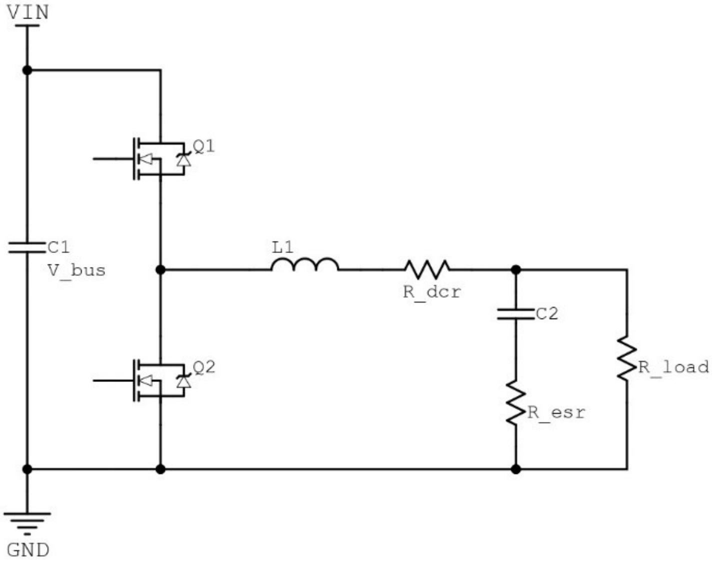

Fig. 1. Basic synchronous buck converter

The primary distinction between non-synchronous and synchronous buck converters lies in the construction of the low-side switch: it is a diode in the non-synchronous variant and a transistor in the synchronous version. In the synchronous buck converter, the allowance for reverse current flow leads to reduced efficiency under light load conditions when compared to its non-synchronous counterpart. Conversely, under heavy load conditions, synchronous buck converters exhibit superior efficiency. This improved efficiency is attributable to the reduced conduction losses in the low-side switching device. Consequently, synchronous buck converters are the preferred choice in applications where the converter is anticipated to predominantly operate under heavy load conditions.

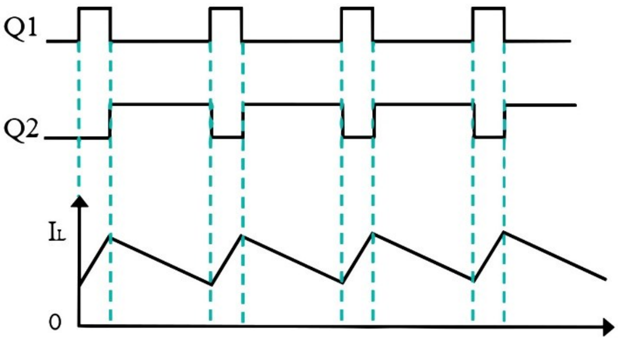

Fig. 2. Synchronous buck converter switching waveforms

In a synchronous buck converter, the primary sources of losses can be categorized as follows:

- Static losses (High and low side switches Rds, inductor active resistance, input and output capacitor losses)
- Dynamic losses (High and low side switch dynamic losses, high side switch output capacitance loss, reverse recovery loss

The control switch duty cycle is defined as follows:

$$D = \frac{V_{out}}{V_{bus}} \tag{1}$$

Where D – is duty cycle, Vout – converter output voltage, Vbus - converter input voltage.

Given a known duty cycle, we can calculate the peak-to-peak inductor current:

$$I_{ripple} = \frac{(V_{bus} - V_{out}) \cdot D}{f_{sw} \cdot L_{out}} \tag{2}$$

Where f_{sw} – working frequency, L_{out} – inductance of L1

The inductor current at turn-on and turn-off is determined using the ripple current and specified output current:

$$I_{L_{\text{turnON}}} = I_{\text{out}} - \frac{I_{\text{ripple}}}{2} \tag{3}$$

$$I_{L_{\text{turnOFF}}} = I_{\text{out}} + \frac{I_{\text{ripple}}}{2} \tag{4}$$

Conduction losses can be estimated by using [4] for a known RMS current:

$$P_{\text{cond\_Q1}} = \left(I_{\text{out}}^2 + \frac{I_{\text{ripple}}^2}{12} \right) \cdot (D - t_{\text{dt1}} \cdot f_{\text{sw}}) \cdot R_{DS(on)\_\text{Q1}} \tag{5}$$

$$P_{\text{cond\_Q2}} = \left(I_{\text{out}}^2 + \frac{I_{\text{ripple}}^2}{12} \right) \cdot (1 - D - t_{\text{dt2}} \cdot f_{\text{sw}}) \cdot R_{\text{DS(on)\_Q2}} \tag{6}$$

Where t_{dt} – specified dead-time, $R_{ds(on)}$ – GaN switch resistance in enabled state

Losses related to C_{oss} (output capacitance) can be estimated using output charge (Q_{oss}) as follows:

$$P_{\text{oss}} = f_{\text{sw}} \cdot E_{\text{oss\_total}} = f_{\text{sw}} \cdot V_{\text{bus}} \cdot Q_{\text{oss}} \tag{7}$$

Reverse conduction losses related to C_{oss} are typically relatively small, as can be confirmed with the following, based on output capacitance for 0V and V_{bus} drain-source voltage:

$$E_{\text{oss\_SD}} = \frac{1}{2} \cdot (C_{\text{OSS(Q1)\_Vbus}} + C_{\text{OSS(Q1)\_0V}}) \cdot V_{\text{sd}}^2 \tag{8}$$

$$P_{\text{oss\_SD}} = 2 \cdot E_{\text{oss\_SD}} \cdot f_{\text{sw}} \tag{9}$$

Here, V_{sd} can be derived from the reverse drain-source characteristics found in the GaN transistor datasheet.

Turn-off transition timings for current are calculated as follows:

$$t_{cr} = \frac{Q_{GS2} \cdot (R_{G_{int}} + R_{G_{ext}} + R_{pu})}{V_{drv\_on} - \left(\frac{V_{GS(th)} + V_{PL}}{2} \right)} \tag{10}$$

Where R_{Gint} is the internal gate resistance of the transistor, R_{Gext} is the external gate resistor, Rpu is the internal pull-up resistance of the gate driver. V_{drv_on} – nominal driver voltage, Q_{gs2} – approximated gate charge for specified current, $V_{gs(th)}$ and V_{pl} – gate threshold and plateau voltages for given GaN FET

Subsequently, the turn-off transition timings for current and voltage are calculated as follows, using driver turn-off voltage (V_{drv_off}, usually, 0V), reverse transfer capacitance (C_{rcc}) and transconductance (g_{fs}), calculated from transfer characteristic:

$$t_{cf} = \frac{Q_{GS2} \cdot (R_{G_{int}} + R_{G_{ext}} + R_{pd})}{\left(\frac{V_{PL} + V_{GS(th)}}{2} \right) - V_{drv\_off}} \tag{11}$$

$$t_{vf} = \left(\frac{Q_{oss\_Q1} + Q_{oss\_Q2}}{V_{drv\_on} - V_{pl}} \right) \cdot \left(\frac{1}{g_{fs}} + \frac{2 \cdot \left(R_{G_{int}} + R_{G_{ext}} + R_{pu} \right) \cdot C_{rss(Q1)\_0V}}{C_{oss(Q1)\_0V} + C_{oss(Q2)\_Vbus}} \right) \tag{12}$$

$$\Delta V_{DS\_cf} = \frac{\frac{1}{2} \cdot t_{cf} \cdot I_{L_{turnOFF}}}{C_{oss(Q1)\_0V} + C_{oss(Q2)\_Vbus}} \tag{13}$$

$$t_{vr} = \frac{Q_{oss\_q1} + Q_{oss\_q2}}{I_{L,turn\_off}} - \frac{t_{cf}}{2} \tag{14}$$

Based on the calculated transition timings, we can estimate the turn-on and turn-off transition losses:

$$P_{ON\_overlap} = f_{sw} \cdot E_{ON\_overlap} = f_{sw} \cdot \frac{1}{2} \cdot V_{BUS} \cdot I_{L_{turnON}} \cdot (t_{cr} + t_{vf}) \tag{15}$$

$$P_{OFF\_overlap} = f_{sw} \cdot E_{OFF\_overlap} = f_{sw} \cdot \frac{1}{6} \cdot t_{cf} \cdot I_{L,turn\_off} \cdot \Delta V_{ds\_cf} \tag{16}$$

Reverse conduction timing and losses can be estimated as follows:

$$t_{on\_SR} = \frac{Q_{GS(th)} \cdot (R_{G_{int}} + R_{G_{ext\_on}} + R_{pu})}{V_{drv\_on} - \left(\dfrac{V_{GS(th)} + V_{drv\_off}}{2}\right)} \tag{17}$$

$$t_{off\_SR} = \frac{2 \cdot Q_{GS(th)} \cdot (R_{G_{int}} + R_{G_{ext\_off}} + R_{pd})}{V_{GS(th)} - V_{drv\_off}} \tag{18}$$

$$t_{SD1} = t_{dt1} - t_{cf} - t_{vr} - \frac{1}{2} \cdot t_{on\_SR} \tag{19}$$

$$t_{SD2} = t_{dt2} - t_{vf} - \frac{1}{2} \cdot t_{cr} - \frac{1}{2} \cdot t_{off\_SR} \tag{20}$$

$$P_{SD} = \left((I_{L,turn\_OFF} \cdot V_{SD} \cdot t_{SD1}) + (I_{L,turn\_ON} \cdot V_{SD} \cdot t_{SD2}) \right) \cdot f_{sw} \tag{21}$$

The gate charge losses for both GaN switches can be calculated in the following way:

$$P_{G\_Q1} = Q_{G\_Q1} \cdot (V_{drv\_on} - V_{drv\_off}) \cdot f_{sw} \tag{22}$$

$$P_{G\_Q2} = Q_{G\_Q2} \cdot (V_{drv\_on} - V_{drv\_off}) \cdot f_{sw} \tag{23}$$

Losses in the windings caused by specified DC resistance of the coil (R_{ind}) of inductors can be calculated based on equations from [5]:

$$P_{L\_winding} = R_{ind} \cdot I_{out}^2 \cdot \left(1 + \frac{1}{12} \left(\frac{I_{ripple}}{I_{out}} \right)^2 \right) \tag{24}$$

Losses related to input and output capacitors can be estimated based on capacitor equivalent series resistance (ESR), as follows:

$$P_{\mathrm{Cin}} = ESR_{\mathrm{Cin}} \cdot I_{\mathrm{out}}^2 \cdot D \cdot (1 - D) \tag{25}$$

$$P_{\mathrm{Cout}} = ESR_{\mathrm{Cout}} \cdot \frac{1}{12} \cdot I_{ripple}^2 \tag{26}$$

The total losses in a GaN FET can be described as follows:

$$P_{Q1} = P_{\mathrm{cond\_Q1}} + P_{\mathrm{oss}} + P_{ON\_\mathrm{overlap}} + P_{OFF\_\mathrm{overlap}} + P_{G\_Q1} \tag{27}$$

$$P_{Q2} = P_{\mathrm{cond\_Q2}} + P_{\mathrm{oss\_sd}} + P_{\mathrm{sd}} + P_{g\_Q2} \tag{28}$$

Losses in the converter can be estimated by considering both the losses in GaN transistors and in passive components:

$$P_{passive} = P_{L\_winding} + P_{Cin} + P_{Cout} \tag{29}$$

$$P_{tot} = P_{Q1} + P_{Q2} + P_{passive} \tag{30}$$

Table 1

Main components losses

Type of loss	Value
Conduction losses in Q1 ($P_{cond\ Q1}$)	0.09 W
C_{oss} related losses (P_{oss})	0.96 W
Turn-on related losses ($P_{on\ overlap}$)	0.39 W
Turn-off related losses ($P_{off\ overlap}$)	0.48 mW
Gate charge losses in Q1 ($P_{G\ Q1}$)	0.01 W
Conduction losses in Q2 ($P_{cond\ Q2}$)	0.27 W
Reverse conduction losses related to C_{oss} ($P_{oss\ sd}$)	6.2 mW
Reverse conduction losses (P_{sd})	0.26 W
Gate charge losses in Q1 ($P_{G\ Q2}$)	0.01 W
Inductor winding losses ($P_{L\ winding}$)	0.31 W
Input capasitor losses (P_{Cin})	0.02 W
Output capacitor losses (P_{Cout})	0.15 mW
Total losses (P_{tot})	2.33W

In the given scenario, a UAV main power supply buck converter operates at a frequency of 1 MHz, providing a maximum current of 10 A to a 12 V load from a 48 V supply. The analysis of hard-switching losses employs the EPC2065 [6] model for both the control switch Q1 and the synchronous rectifier Q2. The converter utilizes an output inductor of 4.7 µH, characterized by a DC series resistance of 3.1 mΩ. Both devices are powered by a 5 V supply and feature zero external gate resistance for both the turn-on and turn-off phases. The gate driver is configured with pull-up and pull-down resistances of 0.7 Ω and 0.4 Ω, respectively. Additionally, a dead time of 12 ns is set for each switching edge. This example will focus on the calculation of the overall losses at a load current of 10 A, using the equations previously introduced. It is important to note that this initial estimation overlooks the effects of parasitic inductances. Calculation results are provided in the table below (Table 1).

Distribution of calculated losses is visualized on Figure 3:

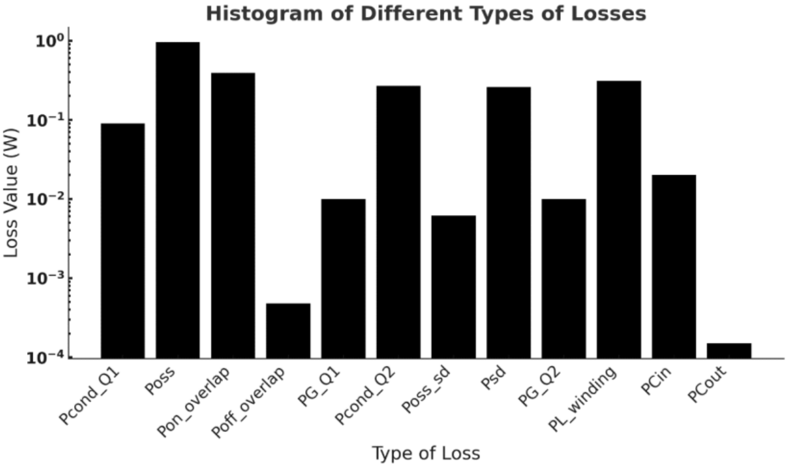

Fig. 3. Synchronous buck converter loss distribution

Overall efficiency can be estimated as:

$$\eta = \frac{I_{out} \cdot V_{out}}{I_{out} \cdot V_{out} + P_{tot}} \cdot 100\% = 98.1\% \qquad (31)$$

Conclusions

This research presents a comprehensive exploration of power loss estimations in compact GaN-based synchronous buck converters, specifically designed for UAV applications. The study underscores the importance of efficient power management in drones to improve flight duration and performance. The insights derived from this study are instrumental in optimizing converter design, achieving a balance between minimizing power loss and preserving essential features such as size, weight, and cost-effectiveness, all critical in UAV systems. This work holds particular significance for engineers and designers in the field of power electronics for UAVs, as it demonstrates the capabilities of GaN technology in enhancing power systems.

During the research, a detailed loss calculation method for synchronous, GaN-based buck converters was proposed, and the main power supply for a UAV was calculated. The proposed design operates at a high frequency of 1 MHz, delivering a maximum current of 10 A to a 12 V load from a 48 V supply, utilizing the EPC2065 GaN transistors. This design achieved an overall theoretical efficiency of 98.1% under full load. Future research directions could include SPICE simulation and physical prototyping of the proposed design.

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